

Designator  
[01] - COVER PAGE.SchDoc

Designator  
[02] - BLOCK DIAGRAM.SchDoc

Designator  
[03] - CONNECTORS

Designator  
[04] - DOC REVISION HISTORY.SchDoc

TEMPLATE NOTES

Set Project Parameters

1) Go to Project -> Project Options -> Parameters  
2) Set Project and Version

Mark Not Fitted Components as

NF

Net Class Example

① Net Class  
ClassName: PCIe

Differential signal example

DIFF100

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Ttitle

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

02A24

Variant: [No Variations]

09/05/2024

V0

DRAFT

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DESIGN CONSIDERATIONS

DESIGN NOTE:  
Example text for informational  
design notes.

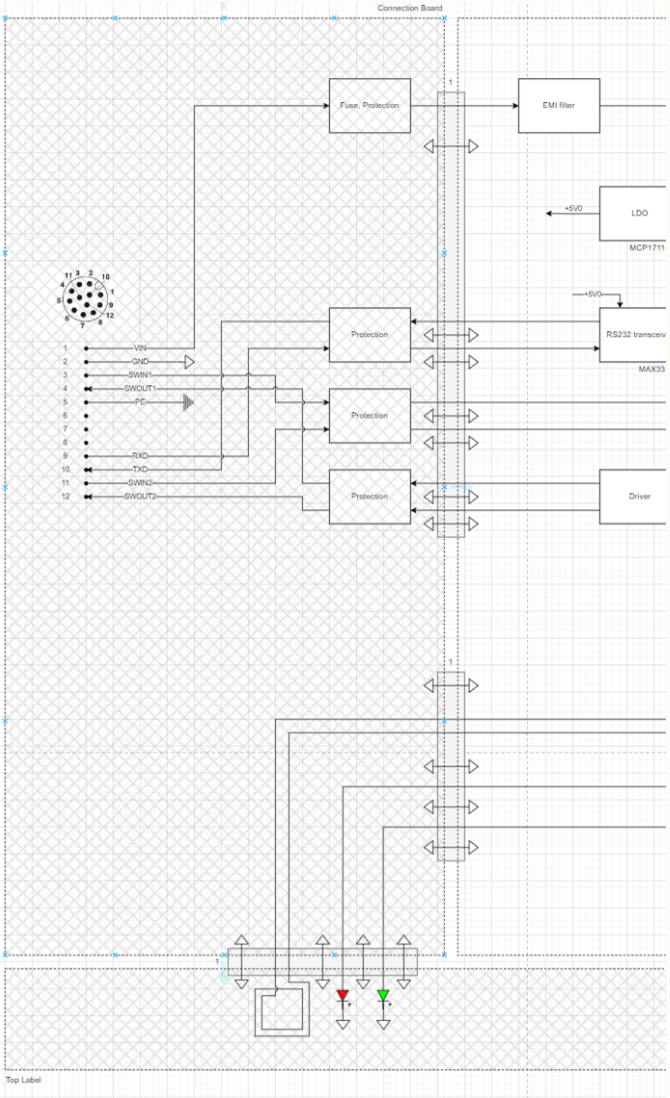
DESIGN NOTE:  
Example text for critical  
design notes.

DESIGN NOTE:  
Example text for cautionary  
design notes.

LAYOUT NOTE:  
Example text for critical  
layout guidelines.

# 02A24

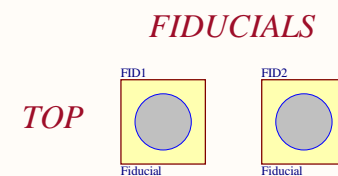
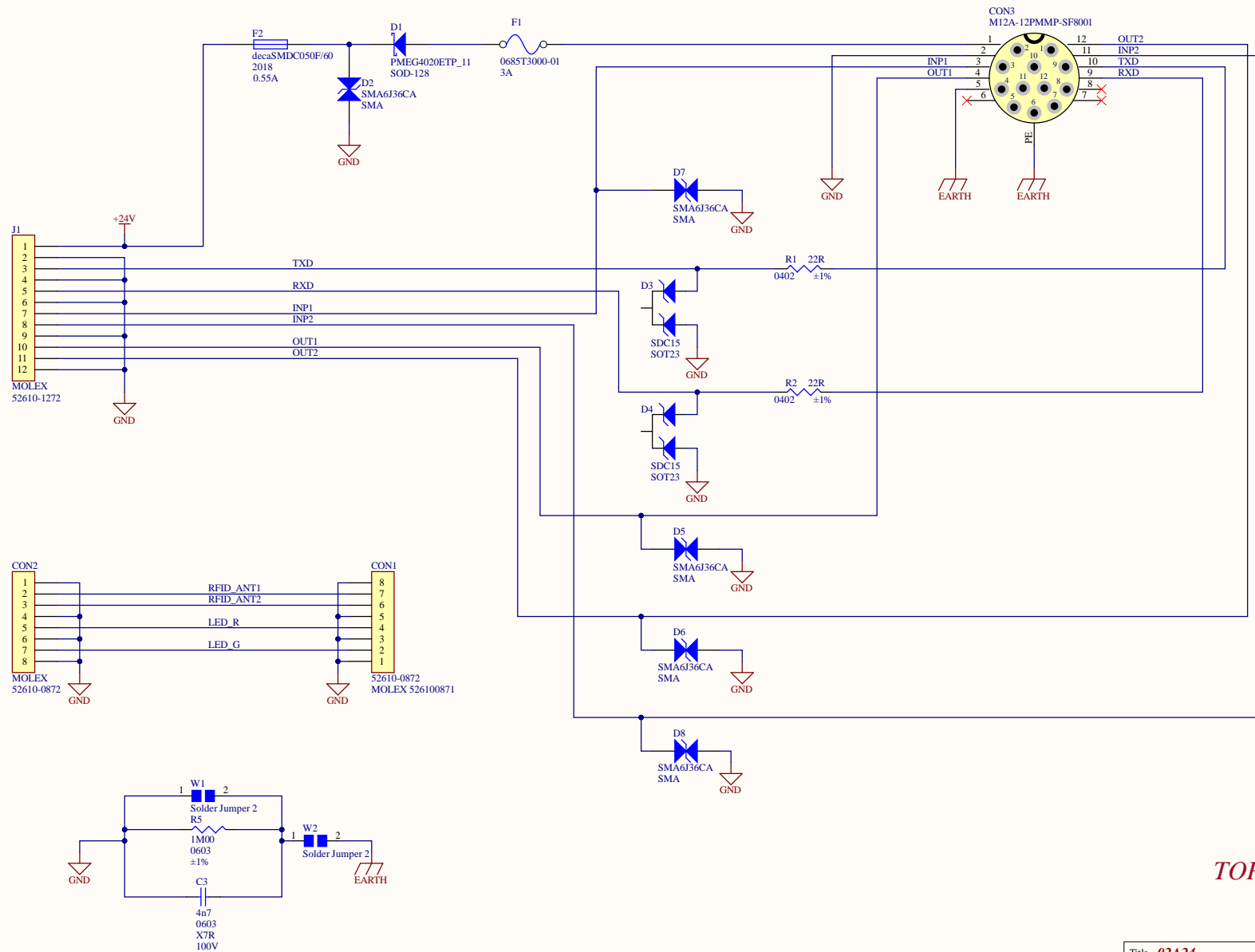
## (Block Diagram)



CLOCK/PE & PDI

# 02A24

## (Connectors)



Title <b>02A24</b>		Kronotech Srl	
Size: <b>A3</b>	Revision: <b>V0</b>	Via Adriatica, 284	
Date: 09/05/2024	Sheet 4 of 5	33030 - Basaldella (UD)	
		Italy	

	1	2	3	4	5	6	7	8
A	<div>DOC: REVISION HISTORY</div>							
B								
C								
D	<div>CLOCKS (CPU &amp; PCIe)</div>							
	1	2	3	4	5	6	7	8

Title <b>02A24</b>		<b>Kronotech Srl</b> <i>Via Adriatica, 284</i> 33030 - Basaldella (UD) <i>Italy</i>	
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